WHAT IS CLAIMED IS:

1. A method comprising:

a memory circuit receiving a data frame to be subsequently transmitted to a destination device via a switching fabric, wherein the data frame comprises header and data fields, and wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

selecting a first multi-bit value [MASK] from a plurality of first multi-bit values according to the data contained in the one of the header fields, wherein the selected first multi-bit value comprises a plurality of bits;

selecting a second multi-bit value [FPOE] from a plurality of second multi-bit values according to the data contained in the one of the header fields, wherein the selected second multi-bit value comprises a plurality of bits;

wherein the bits of each of the first and second multi-bit values corresponds, respectively, to the plurality of data ports;

bit wise logically ANDing the selected first and second multi-bit values to produce a third multi-bit value;

adding the third multi-bit value to a header field of the received data frame;

transmitting the received data frame from the memory circuit to the switching fabric after adding the third multi-bit value to the received data frame;

the data frame exiting the switching fabric through one or more data ports thereof in accordance with the values of the bits of the third multi-bit value.

2. The method of claim 1 wherein the memory circuit is coupled to the switching fabric via a first pair of the plurality of data ports.

3. The method of claim 2 wherein the data frame is transmitted to the switching fabric via one of the first pair of the plurality of data ports.

4. The method of claim 1 wherein the destination device is coupled to the switching fabric via a second pair of the plurality of data ports.

5. The method of claim 4 where the data frame is transmitted to the destination device via one of the second pair of the plurality of data ports.

6. The method of claim 1 wherein each bit of the first multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of the plurality of data ports through which the data frame may exit the switching fabric to reach the destination device.

7. The method of claim 4 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein a first of two bits of the second multi-bit value is set to logical 1, wherein a second of the two bits of the second multi-bit value is set to logical 0, and wherein the two bits correspond, respectively, to the second pair of the plurality of data ports.

8. The method of claim 1 wherein only one bit of the third multi-bit value that is set to logical 1, and wherein the one bit corresponds to a particular data port of the plurality of data ports through which the data frame must exit the switching fabric to reach the destination device.

9. An apparatus comprising:

a memory circuit configured to receive a data frame to be subsequently transmitted to a destination device via a switching fabric, wherein the data frame comprises header and data fields, and wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

a first circuit coupled to the memory circuit, wherein the first circuit is configured to receive data from one of the header fields, and wherein the first circuit is configured to produce a first multi-bit value in response to receiving the data;

a second circuit coupled to the memory circuit, wherein the second circuit is configured to receive the data, and wherein the second circuit is configured to produce a second multi-bit value in response to receiving the data;

a third circuit coupled to the first and second circuits, wherein the third circuit is configured produce a third multi-bit value in response to receiving the first and second multi-bit values from the first and second circuits, respectively, wherein the third circuit is configured to add the third multi-bit to a header field of the data frame;

wherein the memory circuit is configured to transmit the data frame to the switching fabric after the third multi-bit value is added to the header field;

wherein the third multi-bit value identifies one of the plurality of data ports through which the data frame must exit the switching fabric to reach the destination device.

10. The apparatus of claim 9 wherein the memory circuit is coupled to the switching fabric via a first pair of the plurality of data ports.

11. The apparatus of claim 9 further comprising the switching fabric and the destination device, wherein the destination device is coupled to the switching fabric via a second pair of the plurality of data ports.

12. The apparatus of claim 9 wherein each bit of the first multi-bit value is set to logical 1 or logical 0, wherein each bit set to logical 1 corresponds, respectively, to one of the plurality of data ports through which the data frame may exit the switching fabric to reach the destination device.

13. The apparatus of claim 9 wherein each bit of the second multi-bit value is set to logical 1 or logical 0, wherein each bit of the second multi-bit value that is set to logical 1 corresponds to a respective one of the plurality of data ports through which the first data frame may exit the switching fabric to reach one of a plurality of devices coupled to the switching fabric.

14. The apparatus of claim 9 wherein the third circuit is configured to bit wise logically AND the first and second multi-bit values.

15. The apparatus of claim 9 wherein only one bit of the third multi-bit value that is set to logical 1, and wherein the one bit corresponds to a particular data port of the plurality of data ports through which the data frame must exit the switching fabric to reach the destination device.

16. An apparatus comprising:

a buffer configured to receive a data frame to be transmitted to a destination device via a switching fabric, wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

a routing data generation circuit coupled to the buffer, wherein the routing data generation circuit is configured to generate and add routing data to the data frame received by the buffer, wherein the routing data identifies one of the plurality of data ports through which the data frame will exit the switching fabric to reach the destination device;

wherein the buffer is configured to transmit the received data frame to the switching system after the routing data generation circuit adds the routing data to the data frame.

17. The apparatus of claim 16 wherein the buffer is coupled to the switching fabric via first and second data ports thereof.

18. An apparatus comprising:

a memory circuit configured to receive a data frame to be transmitted to a destination device via a switching fabric, wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

means coupled to the memory circuit, to generate and add routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the plurality of data ports through which the data frame will exit the switching fabric to reach the destination device;

wherein the memory circuit is configured to transmit the received data frame to the switching system after the means adds the routing data to the data frame.

19. The apparatus of claim 18 wherein the memory circuit is coupled to the switching fabric via a first pair of the plurality of data ports.

20. A method comprising:

a memory circuit receiving a data frame to be transmitted to a destination device via a switching fabric, wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the plurality of data ports through which the data frame will exit the switching fabric to reach the destination device;

the memory circuit transmitting the received data frame to the switching system after the means adds the routing data to the data frame.

21. A computer readable medium storing instructions executable by a comuter system to implement a method, the method comprising:

a memory circuit receiving a data frame to be transmitted to a destination device via a switching fabric, wherein the switching fabric comprises a plurality of data ports through which data frames enter or exit the switching fabric;

generating and adding routing data to the data frame received by the memory circuit, wherein the routing data identifies one of the plurality of data ports through which the data frame will exit the switching fabric to reach the destination device;

the memory circuit transmitting the received data frame to the switching system after the means adds the routing data to the data frame.